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PTO/SB/05 (1/98)
Approved for use through 09/30/2000. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	2919.1US (96-499.01)
First Inventor or Application Identifier	Pan
Title	Technique for Forming Shallow Trench Isolation Structure without Corner Exposure .....
Express Mail Label No.	EM105821972US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

1 [X] * Fee Transmittal Form *(e.g., PTO/SB/17)* *(Submit an original, and a duplicate for fee processing)*

2 [X] Specification [Total Pages 20]
(preferred arrangement set forth below)
- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings *(if filed)*
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

3. [X] Drawing(s) *(35 U.S.C. 113)* [Total Sheets 4]

4. Oath or Declaration [Total Pages 1]
- a. [ ] Newly executed (original or copy)
- b. [X] Copy from a prior application (37 C.F.R. § 1 63(d)) *(for continuation/divisional with Box 17 completed)* ***[Note Box 5 below]***
  - i [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1 63(d)(2) and 1 33(b)

5 [X] Incorporation By Reference *(useable if Box 4b is checked)* The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. [ ] Microfiche Computer Program *(Appendix)*

7. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
- a. [ ] Computer Readable Copy
- b. [ ] Paper Copy (identical to computer copy)
- c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet & document(s))
9. [ ] 37 C.F.R.§3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [X] Information Disclosure Statement (IDS)/PTO-1449 [X] Copies of IDS Citations
12. [X] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
14. [ ] * Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application, Status still proper and desired
15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [ ] Other: .....

* *A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon*

17. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in a preliminary amendment*

[ ] Continuation [X] Divisional [ ] Continuation-in-part (CIP) of prior application No: 08 / 789,470

Prior application information: Examiner G. Fourson III Group / Art Unit: 2814

18. CORRESPONDENCE ADDRESS

[ ] *Customer Number or Bar Code Label* *(Insert Customer No or Attach bar code label here)* or [ ] *Correspondence address below*

Name	Joseph A. Walkowski				
	Trask Britt & Rossa				
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City	Salt Lake City	State	UT	Zip Code	84110
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Name (Print/Type)	Robert G. Winkle	Registration No. (Attorney/Agent)	37,474
Signature	Robert G. Winkle	Date	5/5/98

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FEE TRANSMITTAL

Patent fees are subject to annual revision on October 1
These are the fees effective October 1, 1997.
Small Entity payments must be supported by a small entity statement, otherwise large entity fees must be paid. See Forms PTO/SB/09-12.

TOTAL AMOUNT OF PAYMENT ($) 916

Complete if Known	
Application Number	
Filing Date	May 5, 1998
First Named Inventor	Pan
Examiner Name	
Group / Art Unit	
Attorney Docket No.	2919.1US

METHOD OF PAYMENT (check one)

1. [X] The Commissioner is hereby authorized to charge indicated fees and credit any over payments to

Deposit Account Number: 20-1469
Deposit Account Name: Trask Britt & Rossa

[X] Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17
[ ] Charge the Issue Fee Set in 37 CFR 1.18 at the Mailing of the Notice of Allowance

2. [X] **Payment Enclosed:**
[X] Check [ ] Money Order [ ] Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	790	201	395	Utility filing fee	790
106	330	206	165	Design filing fee	
107	540	207	270	Plant filing fee	
108	790	208	395	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 790

2. EXTRA CLAIM FEES

		Extra Claims		Fee from below	Fee Paid
Total Claims	22	-20** = 2	X	22	= 44
Independent Claims	4	- 3** = 1	X	82	= 82
Multiple Dependent					=

**or number previously paid, if greater, For Reissues, see below

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	22	203	11	Claims in excess of 20
102	82	202	41	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim, if not paid
109	82	209	41	** Reissue independent claims over original patent
110	22	210	11	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 126

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	400	216	200	Extension for reply within second month	
117	950	217	475	Extension for reply within third month	
118	1,510	218	755	Extension for reply within fourth month	
128	2,060	228	1,030	Extension for reply within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,320	241	660	Petition to revive - unintentional	
142	1,320	242	660	Utility issue fee (or reissue)	
143	450	243	225	Design issue fee	
144	670	244	335	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	790	246	395	Filing a submission after final rejection (37 CFR 1.129(a))	
149	790	249	395	For each additional invention to be examined (37 CFR 1.129(b))	

Other fee (specify) _____

Other fee (specify) _____

* Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($)

SUBMITTED BY

Typed or Printed Name	Robert G. Winkle			Complete (if applicable) Reg. Number	37,474
Signature	Robert G. Winkle	Date	5/5/98	Deposit Account User ID	20-1469

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Pai-Hung Pan

Serial No.: To be assigned

Filed: May 4, 1998

For: TECHNIQUE FOR FORMING SHALLOW TRENCH ISOLATION STRUCTURE WITHOUT CORNER EXPOSURE AND RESULTING STRUCTURE

Examiner: To be assigned

Group Art Unit: To be assigned

Attorney Docket No.: 2919.1US
(96-0499.01)

NOTICE OF EXPRESS MAILING
Express Mail Mailing Label Number:EM105821972US
Date of Deposit with USPS: May 4, 1998
Person mailing Deposit: Timothy W. Ricks

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to examination of the claims on the merits in the above-identified application, please amend this application as follows:

IN THE SPECIFICATION:

Please amend the specification, as follows:

Page 3, line 19, after "filling" delete --,--.

Page 3, line 21, after "of" insert --the--.

Page 4, line 2, change "increases" to --increase--.

Page 5, line 121, change "results" to --result--.

Page 5, line 13, change "604" to --504--.

Page 7, line 8, change "a" to --an--.

Page 7, line 9, change "mixtures" to –mixture--.

Page 7, line 16, change "a" to --an--.

Page 7, line 23, after "122" (1st occur.) insert --is--.

IN THE CLAIMS:

Please amend claims 25, as follows:

Claim 25, line 1, after "on" insert --a--.

Please cancel claims 6-10, 18-24, 29-32 and 39-52.

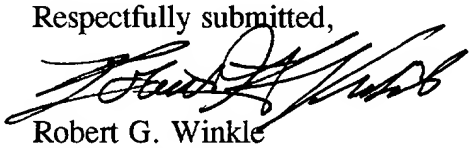
REMARKS

The specification has been amended to correct minor, inadvertent errors. No new subject matter has been introduced with these amendments.

Claims 1-5, 11-17, 25-28 and 33-38 remain in the application. Claim 25 has been amended to a correct minor, inadvertent error. No new subject matter has been introduced with this amendment.

Entry of the above preliminary amendment is respectfully requested. This amendment is submitted prior to the issuance of the first Office action. No new matter has been added.

Respectfully submitted,



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Date: May 5, 1998
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PATENT
Attorney Docket 2919US(96-0499)

CERTIFICATION UNDER 37 C.F R. § 1.10

EM413698670US	01/27/97
Express Mail Mailing Label No.	Date of Deposit

I hereby certify that this application is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. § 1.10 on the date indicated above and is addressed to Commissioner of Patents and Trademarks, Washington, D.C. 20231.

Timothy Ricks	
Typed or printed name of person mailing application	Signature of person mailing application

APPLICATION FOR LETTERS PATENT

for

TECHNIQUE FOR FORMING SHALLOW TRENCH ISOLATION STRUCTURE WITHOUT CORNER EXPOSURE AND RESULTING STRUCTURE

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TECHNIQUE FOR FORMING SHALLOW TRENCH ISOLATION STRUCTURE WITHOUT CORNER EXPOSURE AND RESULTING STRUCTURE

BACKGROUND OF THE INVENTION

Field of the Invention: The present invention relates to an apparatus and method for forming a shallow trench isolation structure. More particularly, the present invention relates to forming the shallow trench isolation structure using a buffer film layer etched such that a capped trench structure is formed which isolates the shallow trench corners.

State of the Art: The semiconductor industry continually strives to increase semiconductor device performance and density by miniaturizing the individual semiconductor components and by miniaturizing the overall semiconductor device dimensions. For example, the semiconductor device density can be increased by more densely integrating the components on the semiconductor chip. However, increasing integration densities by placing the individual circuit elements in closer proximity increases the potential for interactions between the circuit elements. Therefore, it has become necessary to include isolation structures to prevent any significant interaction between circuit elements on the same chip.

Contemporary CMOS technologies generally employ field effect transistors that are adjacent or bounded by trenches. These trenches provide isolation (shallow trench isolation or "STI") for the semiconductor devices. However, the close proximity of each semiconductor device to an edge or corner of the trench may create parasitic leakage paths. The parasitic leakage paths result from an enhancement of the gate electric field near the trench corners. This gate electric field is enhanced by the trench corner's small radius of curvature and the proximity of the gate conductor. As a result of the enhanced gate electric field, the trench corner has a lower threshold voltage (V_t) than the planar portion of the device.

Presently known formation techniques for such trenches generally involve a wet etch, which can exacerbate the parasitic leakage problem by sharpening the trench corners and thinning the gate dielectric near the trench corner. Furthermore, present trench formation techniques generally expose the trench corners before gate electrode deposition. The exposure of trench corners will increase the sub-V_t leakage and degrade gate oxide integrity. The aforementioned problems will be hereinafter referred to collectively as "corner effects."

Corner effects can even dominate on-currents in applications such as DRAM chips that require narrow channel widths to achieve high density. This parallel current-carrying corner effect becomes the dominant MOSFET contributor to standby current in low standby power logic applications and to leakage in DRAM cells. Furthermore, there exists concern that the enhanced electric fields due to field crowding at the trench corner may impact dielectric integrity.

Numerous techniques have been proposed to overcome the above discussed corner effects. Commonly-owned U.S. Patent 5,433,794 issued July 18, 1995 to Fazan et al., hereby incorporated herein by reference, and U.S. Patent 5,521,422 issued May 28, 1996 to Mandelman et al., each teach forming shallow trench isolation structures wherein insulating material spacers are formed abutting the trench corners and the isolating material filling, and extending above the trench. When a wet pad oxide etch is performed, the isolating material combines with the spacers to form an isolation trench having a dome or cap-like covering the peripheral edges of trench which substantially overcomes the corner effects and consequential leakage between active areas on the substrate. Although the techniques taught in these patents are effective in minimizing corner effects, the techniques require additional fabrication steps which increase the overall cost of the semiconductor component.

U.S. Patent 5,436,488 issued July 25, 1995 to Poon et al. teaches improving trench isolation by increasing the thickness of the gate dielectric overlying the trench corner between the substrate and gate electrode. However, the process taught in this

patent also requires numerous additional fabrication steps and structures, which of course increases the overall cost of the semiconductor component.

Therefore, it would be advantageous to develop a shallow isolation trench and a technique for forming the trench which substantially eliminates the aforementioned corner effects, while using inexpensive, commercially-available, widely-practiced semiconductor device fabrication techniques and apparatus.

SUMMARY OF THE INVENTION

The present invention relates to a shallow isolation trench structure which is formed using a buffer film layer. The buffer film layer is etched in such a manner that an isolation material within the shallow trench has a cap which covers the shallow trench corners to prevent corner effects.

The method of the present invention comprises providing a semiconductor substrate, preferably a silicon substrate, with a dielectric layer, preferably silicon dioxide, formed on at least one surface of the semiconductor substrate to a thickness of between 50 and 300Å. The dielectric layer can be formed by any known technique, including thermally oxidizing the surface of the semiconductor substrate, chemical vapor deposition, sputtering, or the like. A buffer film layer, preferably silicon nitride, is then formed over the dielectric layer by any known deposition technique, preferably chemical vapor deposition. Although silicon nitride is preferred, the buffer layer may be any known material which is oxidation resistant and can be etched selectively to oxide films.

A photoresist mask is applied and patterned on the buffer film layer. The buffer film layer, the dielectric layer, and semiconductor substrate are then etched either simultaneously with a non-selective etch or in steps with selective etches to form a shallow trench with sidewalls and a bottom. The photoresist mask is then removed to form a trenched structure.

After stripping the photoresist and cleaning the trenched structure, a thin layer of oxide, between about 50 and 150Å thick, is grown on the shallow trench sidewalls and bottom, preferably by thermal oxidization. The buffer film layer is then selectively etched horizontally and vertically to move the buffer film layer back from the shallow trench. The purpose for using a buffer film layer, which is oxidation resistant, as discussed above, is shown in FIG. 11. If an oxidizable material is used as a buffer film layer 202 over a dielectric layer 204 and a substrate 206, the formation of a thin oxide layer 208 in trench 210 would also cause the formation of an additional thin layer of oxide 212 to form on the buffer film layer 202. Most oxidizable materials, such as silicon dioxide, used for forming the buffer film layer 202 have a greater affinity for growing oxides than the semiconductor substrate. As a results, the additional thin oxide layer 212 is relatively thicker than the thin oxide layer 208, which results in a narrowing of the opening at the mouth of the trench 210. This narrowing makes it difficult to fill the trench 210 with an isolation material 214, and may even cause the formation of voids 216 in the isolation material 214 during the application of the isolation material 214.

In the method of the present invention, after etching back the buffer film layer, the shallow trench is then filled with an isolation material. The resulting structure is preferably annealed to densify the deposited isolation material. Densification of the deposited isolation material is required to enhance the resistance of the isolation material to etching during subsequent processing. A portion of the isolation material over the buffer film layer is then removed to the level of the buffer film layer. The removal of isolation material is preferably achieved with a process such as chemical mechanical planarization which abrades away the isolation material down to the buffer film layer. The buffer film layer is then selectively etch away to form an isolation structure. When this isolation structure is etched during a subsequent wet oxide etch process, the isolation structure will form the capped shallow trench isolation structure

which covers the trench corners. This capped shallow trench isolation structure substantially minimizes corner effects.

BRIEF DESCRIPTION OF THE DRAWINGS

While the specification concludes with claims particularly pointing out and distinctly claiming that which is regarded as the present invention, the advantages of this invention can be more readily ascertained from the following description of the invention when read in conjunction with the accompanying drawings in which:

FIGS. 1-10 are cross-sectional views of the method of forming a shallow trench isolation structure of the present invention; and

FIG. 11 is a cross-sectional view of a shallow trench isolation structure formed with a conventional oxidizable buffer film layer.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIGS. 1 through 10 illustrate, in cross-section, a method for forming a shallow trench isolation structure in accordance with one embodiment of the present invention. As shown in FIG. 1, the method comprises forming a layered structure 100 of a semiconductor substrate 102, a dielectric layer 104, and a buffer film layer 106. The semiconductor substrate 102 preferably includes silicon and the dielectric layer 104 preferably includes silicon dioxide. The dielectric layer 104 is preferably between 50 and 300Å thick (a convenient range for process integration) and can be formed by any known technique including thermally oxidizing the surface of the semiconductor substrate 102, chemical vapor deposition, sputtering, or the like. The buffer film layer 106, preferably comprising silicon nitride, is formed over the dielectric layer 104 by any known deposition technique, preferably chemical vapor deposition.

A photoresist mask 108, either positive or negative resist (preferably positive) as known in the art, is applied over the buffer film layer 106 and patterned using standard photolithographic patterning techniques, as shown in FIG. 2. The buffer film layer 106

and the dielectric layer 104 are then etched by standard etching techniques to form patterned recess 110, as shown in FIG. 3. The silicon substrate 102 is then dry etched to form a shallow trench 112 with sidewalls 114 and a bottom 116, seen in FIG. 4. It is, of course, understood that the buffer film layer 106, the dielectric layer 104, and semiconductor substrate 102 can be etched in one non-selective etching step. The photoresist mask 108 is removed using standard photoresist stripping techniques, preferably by plasma etch, to form a trenched structure 118, as shown in FIG. 4.

After stripping the photoresist and cleaning (preferably with a H_2O_2/H_2SO_4 or H_2O_2/HCl mixtures) the trenched structure 118, a thin layer of oxide 120, between about 50 and 150Å thick, is grown on the shallow trench sidewalls 114 and the shallow trench bottom 116, preferably by thermal oxidization, as shown in FIG. 5. As shown in FIG. 6, the buffer film layer 106 is then selectively etched horizontally and vertically to move the buffer film layer 106 back from the shallow trench 112. The etching of the buffer film layer 106 is preferably a wet etch process including an application of a 100:1 HF (hydrofluoric acid) solution followed by an application of a H_3PO_4 (phosphoric acid) solution or a H2O/N$(CH_2CH_3)_4$OH ("TMAH") solution.

The shallow trench 112 is then filled with an isolation material 122, as shown in FIG. 7. The isolation material 122 is preferably silicon dioxide deposited by any known technique including chemical vapor deposition using tetraethylorthosilane (TEOS) or ozone as source gases, electron cyclotron resonance deposition, spin-on deposition, and the like. Optionally, the isolation material 122 can be annealed to densify the deposited isolation material 122. Densification of the deposited isolation material 122 used to enhance the resistance of the isolation material 122 to etching during subsequent processing. The annealing is preferably conducted in a nitrogen or other inert gas atmosphere to prevent oxidation of the semiconductor substrate 102 beneath the isolation material 122.

As shown in FIG. 8, the isolation material 122 is removed down to the buffer film layer 106, preferably by a mechanical abrasion process, such as

chemical/mechanical planarization. The buffer film layer 106 is then selectively etched away, by any known technique such as a hot H_3PO_4 (phosphoric acid), to form an isolation structure 124, as shown in FIG. 9. When this isolation structure 124 is etched during a subsequent wet oxide process to expose the upper surface 132 of said semiconductor substrate 102, the isolation structure 124 will form a capped shallow trench isolation structure 126 which covers the trench corners 128 of the shallow trench 112 with ledges 130, as shown in FIG. 10. The ledges 130 preferably extend horizontally between about 50 and 150Å from the trench corners 128. These ledges 130 prevent the aforementioned corner effects.

* * * * *

Having thus described in detail preferred embodiments of the present invention, it is to be understood that the invention defined by the appended claims is not to be limited by particular details set forth in the above description, as many apparent variations are possible without departing from the spirit or scope thereof.

CLAIMS

What is claimed is:

1. A method of forming an isolation structure for a semiconductor device, comprising:

providing a layered structure comprising a semiconductor substrate, a dielectric layer, and a buffer film layer;

etching said layered structure through said buffer film layer, through said dielectric layer, and into said semiconductor substrate to define a trench having sidewalls and a bottom;

forming an oxide layer on exposed portions of said semiconductor substrate within said trench;

selectively etching a portion of said buffer film layer;

applying a layer of isolation material over said buffer film layer to fill said trench;

removing a portion of said isolation material layer above said buffer film layer; and

removing said buffer film layer.

2. The method of claim 1, wherein forming said oxide layer includes thermal oxidation of said exposed portions of said semiconductor substrate within said trench.

3. The method of claim 1, wherein selectively etching said portion of said buffer film layer includes horizontal and vertical etching of said buffer film layer.

4. The method of claim 3, wherein selectively etching said buffer film layer portion results in a portion of said buffer film layer remaining on said semiconductor substrate and extending a predetermined distance from said trench.

5. The method of claim 1, further including annealing said isolation material layer.

6. An isolation structure for a semiconductor device formed by the method comprising:

providing a layered structure comprising a semiconductor substrate, a dielectric layer, and a buffer film layer;

etching said layered structure through said buffer film layer, through said dielectric layer, and into said semiconductor substrate to define a trench having sidewalls and a bottom;

forming an oxide layer on exposed portions of said semiconductor substrate within said trench;

selectively etching a portion of said buffer film layer;

applying a layer of isolation material over said buffer film layer to fill said trench;

removing a portion of said isolation material layer above said buffer film layer; and

removing said buffer film layer.

7. The isolation structure of claim 6, wherein forming said oxide layer includes thermal oxidation of said exposed portions of said semiconductor substrate within said trench.

8. The isolation structure of claim 6, wherein selectively etching said portion of said buffer film layer includes horizontal and vertical etching of said buffer film layer.

9. The isolation structure of claim 8, wherein selectively etching said buffer film layer portion results in a portion of said buffer film layer remaining on said semiconductor substrate and extending a predetermined distance from said trench.

10. The isolation structure of claim 6, formed by a method further comprising annealing said isolation material layer.

11. A method of forming a capped shallow trench isolation structure for a semiconductor device, comprising:

providing a layered structure comprising a semiconductor substrate, a dielectric layer, and a buffer film layer;

etching said layered structure through said buffer film layer, through said dielectric layer, and into said semiconductor substrate to define a trench having sidewalls and a bottom;

forming an oxide layer on exposed portions of said semiconductor substrate within said trench sidewalls and said trench bottom;

selectively etching a portion of said buffer film layer to expose opposing trench edges at an intersection of said trench sidewalls and an upper surface of said semiconductor substrate;

applying a layer of isolation material over said buffer film layer to fill said trench;

removing a portion of said isolation material layer above said buffer film layer;

removing said buffer film layer; and

etching said isolation material to form said capped shallow trench isolation structure.

12. The method of claim 11, wherein forming said oxide layer includes thermal oxidation of said exposed portions of said semiconductor substrate within said trench.

13. The method of claim 11, wherein selectively etching said portion of said buffer film layer includes horizontal and vertical etching of said buffer film layer.

14. The method of claim 13, wherein selectively etching said buffer film layer portion results in a portion of said buffer film layer remaining on said semiconductor substrate and extending a predetermined distance from said trench.

15. The method of claim 11, further including annealing said isolation material layer.

16. The method of claim 11, wherein said capped shallow trench isolation structure includes ledges which extend a predetermined distance over said upper surface of said semiconductor substrate adjacent said opposing trench edges.

17. The method of claim 16, wherein said ledges extend over said upper surface of said semiconductor substrate between about 50 and 150Å.

18. A capped shallow trench isolation structure formed by the method comprising:

providing a layered structure comprising a semiconductor substrate, a dielectric layer, and a buffer film layer;

etching said layered structure through said buffer film layer, through said dielectric layer, and into said semiconductor substrate to define a trench having sidewalls and a bottom;

forming an oxide layer on exposed portions of said semiconductor substrate within said trench sidewalls and said trench bottom;

selectively etching a portion of said buffer film layer to expose opposing trench edges at an intersection of said trench sidewalls and an upper surface of said semiconductor substrate;

applying a layer of isolation material over said buffer film layer to fill said trench;

removing a portion of said isolation material layer above said buffer film layer;

removing said buffer film layer; and

etching said isolation material to form said capped shallow trench isolation structure.

19. The capped shallow trench isolation structure of claim 18, wherein forming said oxide layer includes thermal oxidation of said exposed portions of said semiconductor substrate within said trench.

20. The capped shallow trench isolation structure of claim 18, wherein selectively etching said portion of said buffer film layer includes horizontal and vertical etching of said buffer film layer.

21. The capped shallow trench isolation structure of claim 20, wherein selectively etching said buffer film layer portion results in a portion of said buffer film layer remaining on said semiconductor substrate and extending a predetermined distance from said trench.

22. The capped shallow trench isolation structure of claim 18, formed by a method comprising annealing said isolation material layer.

23. The capped shallow trench isolation structure of claim 18, wherein said capped shallow trench isolation structure includes ledges which extend a predetermined distance over said upper surface of said semiconductor substrate adjacent said opposing trench edges.

24. The capped shallow trench isolation structure of claim 23, wherein said ledges extend over said semiconductor substrate between about 50 and 150Å.

25. A method of forming an isolation structure on semiconductor device layered structure including a semiconductor substrate, a dielectric layer, and a buffer film layer, said layered structure including a trench through said buffer film layer, said dielectric layer, and into said semiconductor substrate, wherein an oxide layer is formed on exposed portions of said semiconductor substrate within said trench, comprising:

selectively etching a portion of said buffer film layer;

applying a layer of isolation material over said buffer film layer to fill said trench;

removing a portion of said isolation material layer above said buffer film layer; and

removing said buffer film layer.

26. The method of claim 25, wherein selectively etching said portion of said buffer film layer includes horizontal and vertical etching of said buffer film layer.

27. The method of claim 26, wherein selectively etching said buffer film layer portion results in a portion of said buffer film layer remaining on said semiconductor substrate and extending a predetermined distance from said trench.

28. The method of claim 25, further including annealing said isolation material layer.

29. An isolation structure for a semiconductor device layered structure including a semiconductor substrate, a dielectric layer, and a buffer film layer, said layered structure including a trench through said buffer film layer, said dielectric layer, and into said semiconductor substrate, wherein an oxide layer is formed on exposed portions of said semiconductor substrate within said trench, formed by the method comprising:

selectively etching a portion of said buffer film layer;

applying a layer of isolation material over said buffer film layer to fill said trench; removing a portion of said isolation material layer above said buffer film layer; and removing said buffer film layer.

30. The isolation structure of claim 29, wherein selectively etching said portion of said buffer film layer includes horizontal and vertical etching of said buffer film layer.

31. The isolation structure of claim 30, wherein selectively etching said buffer film layer portion results in a portion of said buffer film layer remaining on said semiconductor substrate and extending a predetermined distance from said trench.

32. The isolation structure of claim 29, formed by a method further comprising annealing said isolation material layer.

33. A method of forming a capped shallow trench isolation structure for a semiconductor device layered structure including a semiconductor substrate, a dielectric layer, and a buffer film layer, said layered structure including a trench through said buffer film layer, said dielectric layer, and into said semiconductor substrate, wherein an oxide layer is formed on exposed portions of said semiconductor substrate within said trench, comprising:

selectively etching a portion of said buffer film layer to expose opposing trench edges at an intersection of said trench and an upper surface of said semiconductor substrate;

applying a layer of isolation material over said buffer film layer to fill said trench;

removing a portion of said isolation material layer above said buffer film layer;

removing said buffer film layer; and

etching said isolation material to form said capped shallow trench isolation structure.

34. The method of claim 33, wherein selectively etching said portion of said buffer film layer includes horizontal and vertical etching of said buffer film layer.

35. The method of claim 34, wherein selectively etching said buffer film layer portion results in a portion of said buffer film layer remaining on said semiconductor substrate and extending a predetermined distance from said trench.

36. The method of claim 33, further including annealing said isolation material layer.

37. The method of claim 33, wherein said capped shallow trench isolation structure includes ledges which extend a predetermined distance over said upper surface of said semiconductor substrate adjacent said opposing trench edges.

38. The method of claim 37, wherein said ledges extend over said upper surface of said semiconductor substrate between about 50 and 150Å.

39. A capped shallow trench isolation structure for a semiconductor device layered structure including a semiconductor substrate, a dielectric layer, and a buffer film layer, said layered structure including a trench through said buffer film layer, said dielectric layer, and into said semiconductor substrate, wherein an oxide layer is formed on exposed portions of said semiconductor substrate within said trench, formed by the method comprising:

selectively etching a portion of said buffer film layer to expose opposing trench edges at an intersection of said trench and an upper surface of said semiconductor substrate;

applying a layer of isolation material over said buffer film layer to fill said trench;
removing a portion of said isolation material layer above said buffer film layer;
removing said buffer film layer; and
etching said isolation material to form said capped shallow trench isolation structure.

40. The capped shallow trench isolation structure of claim 39, wherein selectively etching said portion of said buffer film layer includes horizontal and vertical etching of said buffer film layer.

41. The capped shallow trench isolation structure of claim 40, wherein selectively etching said buffer film layer portion results in a portion of said buffer film layer remaining on said semiconductor substrate and extending a predetermined distance from said trench.

42. The capped shallow trench isolation structure of claim 39, formed by a method comprising annealing said isolation material layer.

43. The capped shallow trench isolation structure of claim 39, wherein said capped shallow trench isolation structure includes ledges which extend a predetermined distance over said upper surface of said semiconductor substrate adjacent said opposing trench edges.

44. The capped shallow trench isolation structure of claim 43, wherein said ledges extend over said semiconductor substrate between about 50 and 150Å.

45. A shallow trench isolation structure, having integral ledges which extend a predetermined distance from a trench formed in a semiconductor device layered structure including a semiconductor substrate, a dielectric layer, and a buffer film

layer, said trench extending through said buffer film layer, said dielectric layer, and into said semiconductor substrate, formed by the method comprising:

forming an oxide layer on exposed portions of said semiconductor substrate within said trench;

selectively etching a portion of said buffer film layer to expose opposing trench edges at an intersection of said trench and an upper surface of said semiconductor substrate;

applying a layer of isolation material over said buffer film layer to fill said trench;

removing a portion of said isolation material layer above said buffer film layer;

removing said buffer film layer; and

etching said isolation material to form said capped shallow trench isolation structure.

46. The shallow trench isolation structure of claim 45, wherein forming said oxide layer includes thermal oxidation of said exposed portions of said semiconductor substrate within said trench.

47. The shallow trench isolation structure of claim 45, wherein selectively etching said portion of said buffer film layer includes horizontal and vertical etching of said buffer film layer.

48. The shallow trench isolation structure of claim 47, wherein selectively etching said buffer film layer portion results in a portion of said buffer film layer remaining on said semiconductor substrate and extending a predetermined distance from said trench.

49. The shallow trench isolation structure of claim 45, formed by a method comprising annealing said isolation material layer.

50. The shallow trench isolation structure of claim 45, wherein said ledges extend over said semiconductor substrate between about 50 and 150Å.

51. A capped shallow trench isolation structure comprising a homogenous isolation material disposed within a trench in a semiconductor substrate, wherein said homogenous isolation material includes ledges which extend a predetermined distance over an upper surface of said semiconductor substrate from said trench.

52. The capped shallow trench isolation structure of claim 51, wherein said ledges extend over said semiconductor substrate between about 50 and 150Å from said trench.

ABSTRACT

A shallow isolation trench structure and methods of forming the same wherein the method of formation comprises a layered structure of a buffer film layer over a dielectric layer which is atop a semiconductor substrate. The buffer film layer comprises a material which is oxidation resistant and can be etched selectively to oxide films. The layered structure is patterned with a resist material and etched to form a shallow trench. A thin oxide layer is formed in the trench and the buffer film layer is selectively etched to move the buffer film layer back from the corners of the trench. An isolation material is then used to fill the shallow trench and the buffer film layer is stripped to form an isolation structure. When the structure is etched by subsequent processing step(s), a capped shallow trench isolation structure which covers the shallow trench corners is created.

FIG 1

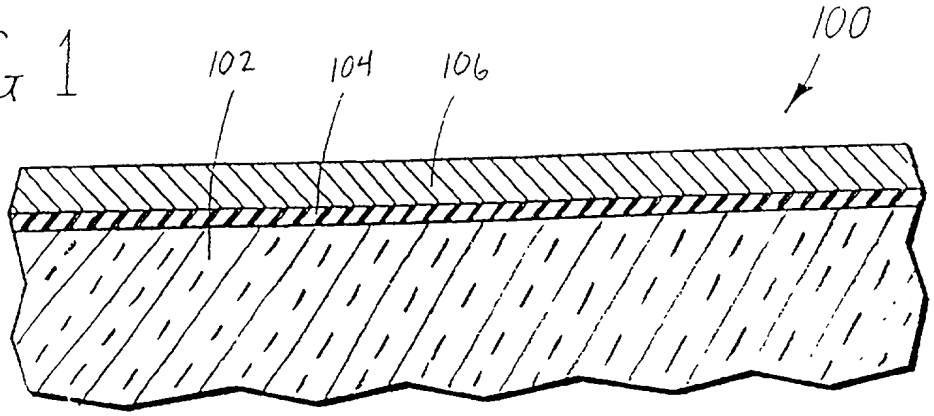


FIG. 2

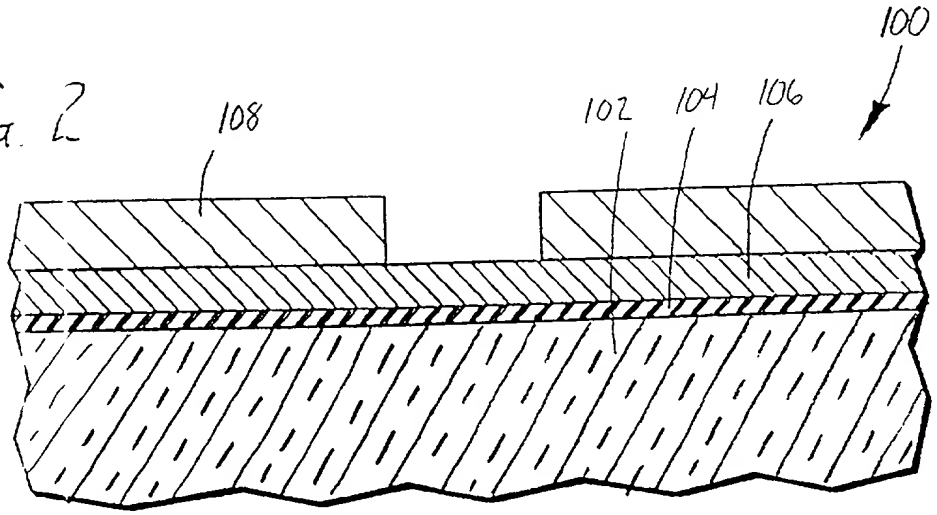


FIG. 3

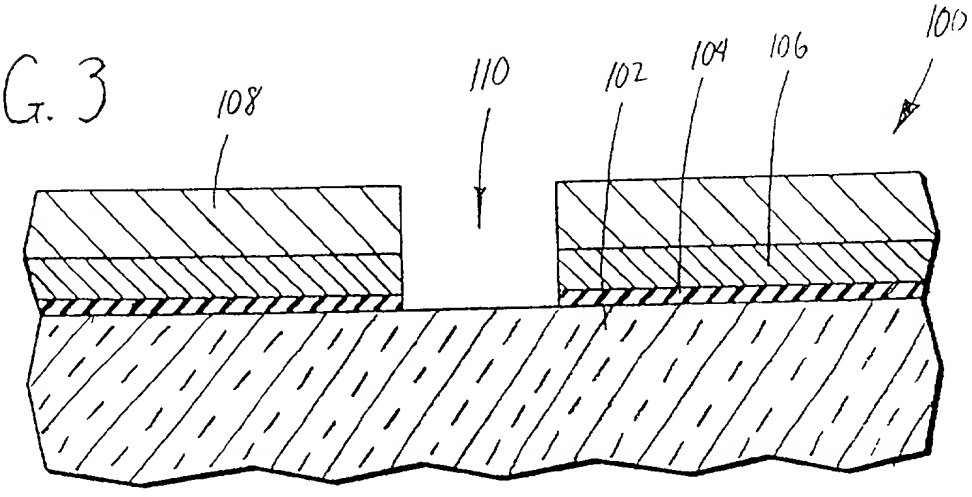


FIG. 4

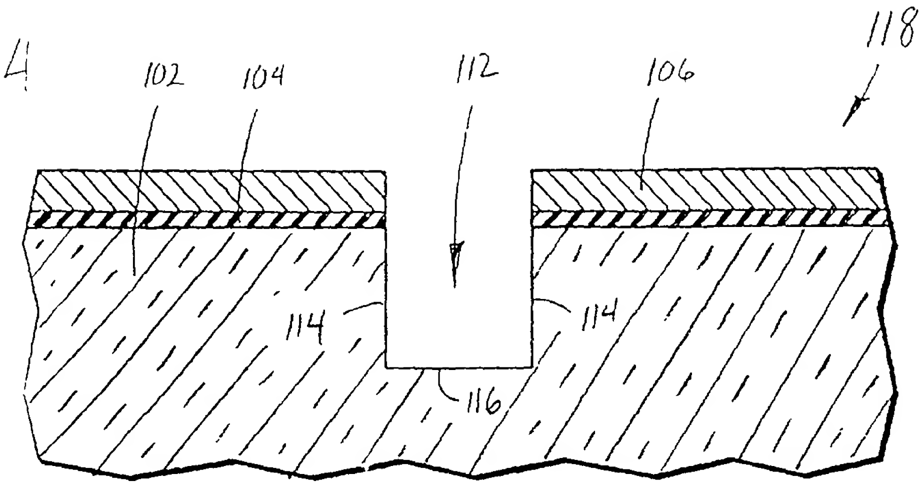


FIG. 5

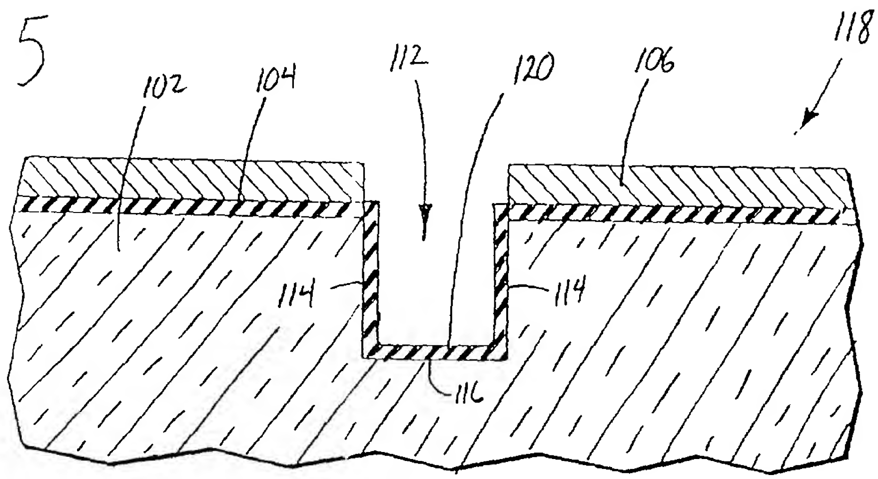


FIG. 6

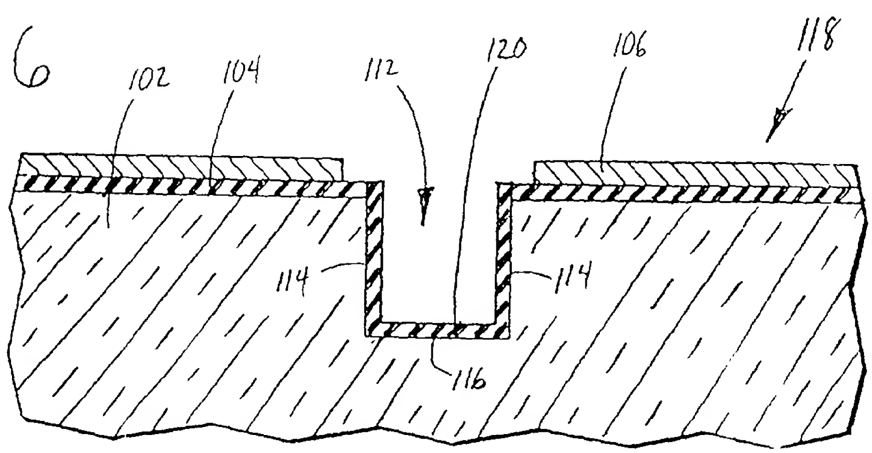


FIG. 7

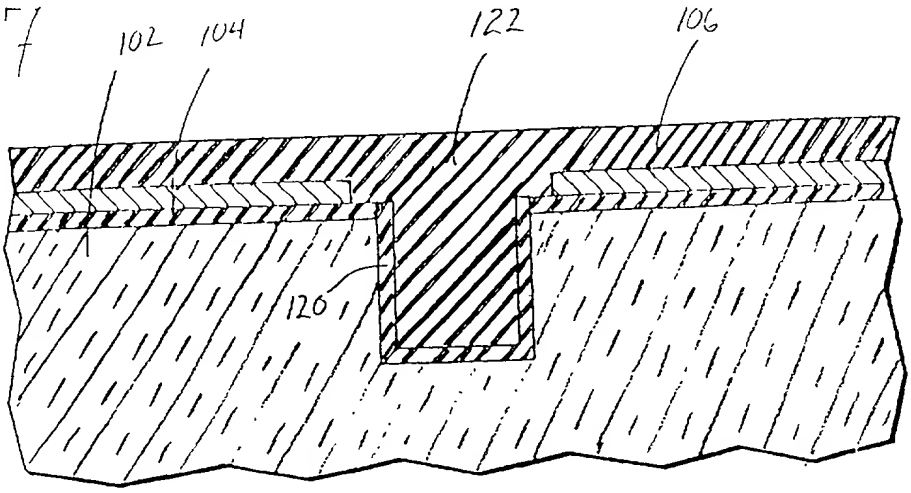


FIG. 8

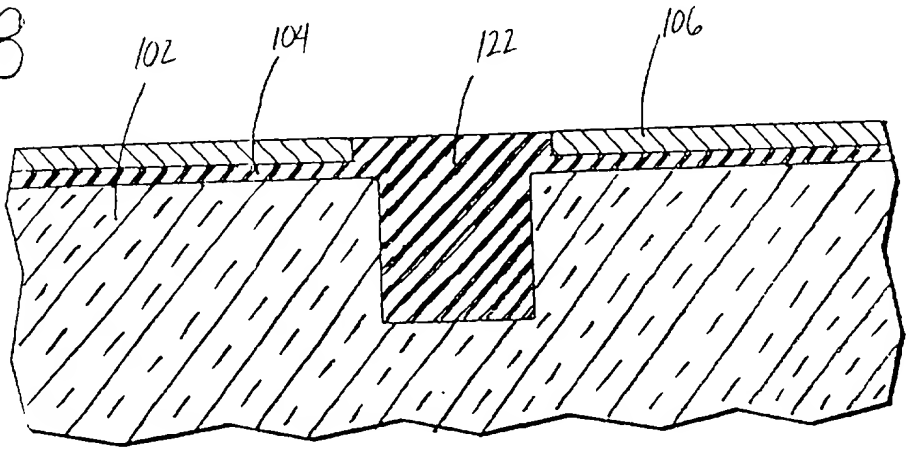


FIG. 9

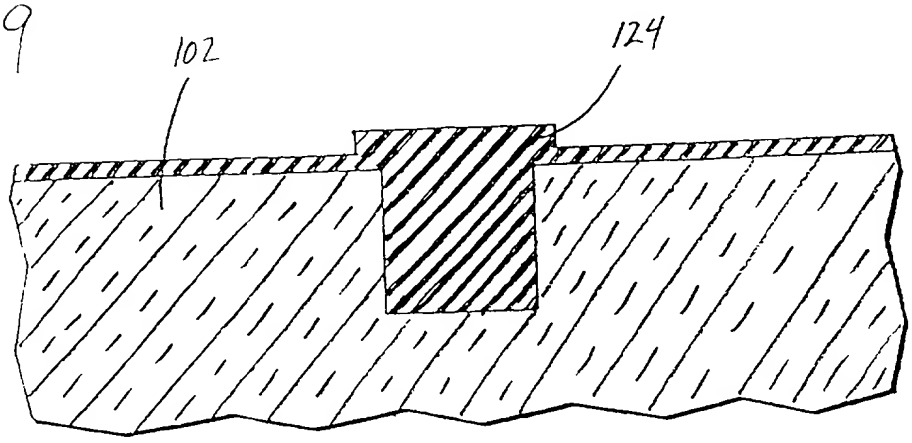


FIG. 10

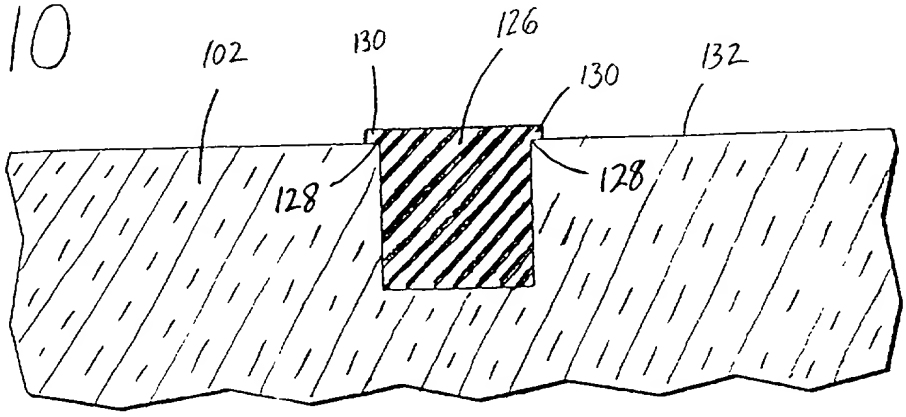
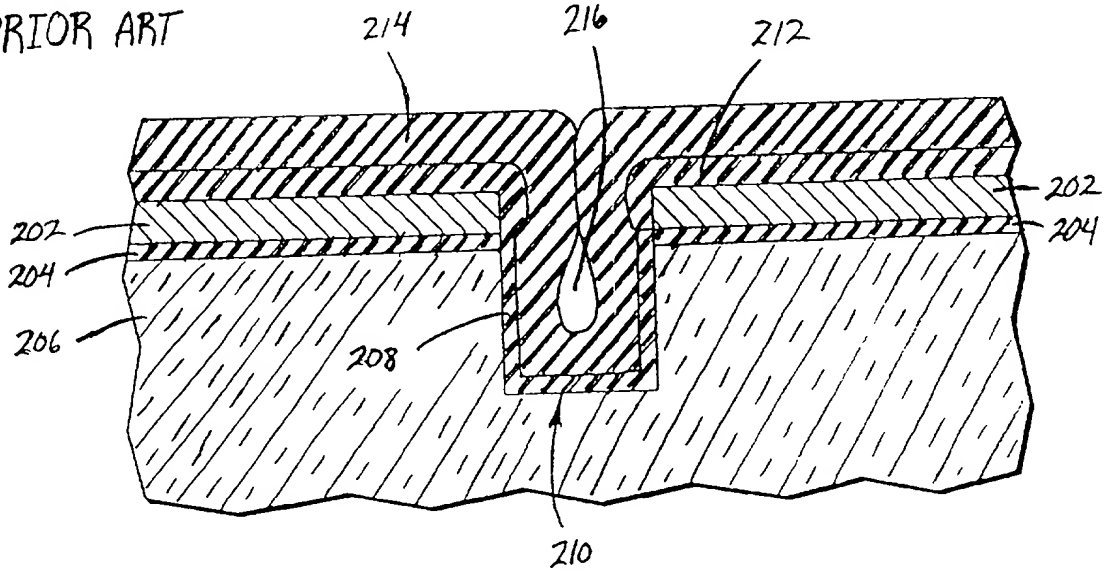


FIG. 11

PRIOR ART



DECLA' TION FOR PATENT APPLICATION (WITH POWF 'F ATTORNEY)

As an inventor named below or on any attached continuation page, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name.

I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **TECHNIQUE FOR FORMING SHALLOW TRENCH ISOLATION STRUCTURE WITHOUT CORNER EXPOSURE AND RESULTING STRUCTURE**, the specification of which (check one):

- ☒ is attached hereto.
- ☐ was filed on _____ as United States application serial no. _____ and was amended on _____.
- ☐ was filed on _____ as PCT international application no _____ and was amended under PCT Article 19 on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to the patentability of the subject matter claimed in this application, as "materiality" is defined in Title 37, Code of Federal Regulations § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 (a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate or § 365(a) of any PCT international application(s) designating at least one country other than the United States of America listed below and on any attached continuation page and have also identified below and on any attached continuation page any foreign application for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America having a filing date before that of the application(s) on which priority is claimed.

Prior foreign/PCT application(s):

				Priority Claimed	
_____ (number)	_____ (country)	_____ (day/month/year filed)		Yes	No
_____ (number)	_____ (country)	_____ (day/month/year filed)		Yes	No

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or § 365(c) of PCT international application(s) designating the United States of America listed below and on any attached continuation page and, insofar as the subject matter of each of the claims of this application is not disclosed in any such prior application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations § 1.56 which became available between the filing date of such prior application and the national or PCT international filing date of this application:

_____ (application serial no.)	_____ (filing date)	_____ (status - pending, patented or abandoned)
_____ (application serial no.)	_____ (filing date)	_____ (status - pending, patented or abandoned)

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

_____ (provisional application no.)	_____ (filing date)
_____ (provisional application no.)	_____ (filing date)
_____ (provisional application no.)	_____ (filing date)

I hereby appoint the following Registered Practitioners to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole inventor: Pai Hung Pan
Inventor's signature _____ Date 01/23/97
Residence: Boise, Idaho
Citizenship: U.S.A.
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